Q8F202C32/Q8F203C32
1T 8051-based 32K Microcontroller

FEATURES

Core and System	
8051	• Fully static design 8-bit high performance 1T 8051-based CMOS microcontroller. • Instruction set fully compatible with MCS-51. • 4-priority-level interrupts capability. • Dual Data Pointers (DPTRs).
Power on Reset (POR)	• POR with 1.15V threshold voltage level
Brown-out Detector (BOD)	• 4-level selection, with brown-out interrupt and reset option. (4.4V / 3.7V / 2.7V / 2.2V)
Low Voltage Reset (LVR)	• LVR with 2.0V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID) • 128-bytes security protection memory SPROM
Memories	
Flash	• Up to 32 KBytes of APROM for User Code. • 4/3/2/1 Kbytes of Flash for loader (LDROM) configure from APROM for In-System-Programmable (ISP) • Flash Memory accumulated with pages of 128 Bytes from APROM by In-Application-Programmable (IAP) means whole APROM can be use as Data Flash • An additional 128 bytes security protection memory SPROM • Code lock for security by CONFIG
SRAM	• 256 Bytes on-chip RAM. • Additional 2 KBytes on-chip auxiliary RAM (XRAM) accessed by MOVX instruction.
Clocks	
External Clock Source	• 4~24 MHz High-speed external crystal oscillator (HXT) for precise timing operation
Internal Clock Source	• Default 16 MHz high-speed internal oscillator (HIRC) trimmed to ±1% (accuracy at 25 ˚C, 3.3 V), ±2% in -20~105˚C. • Selectable 24 MHz high-speed internal oscillator (HIRC).

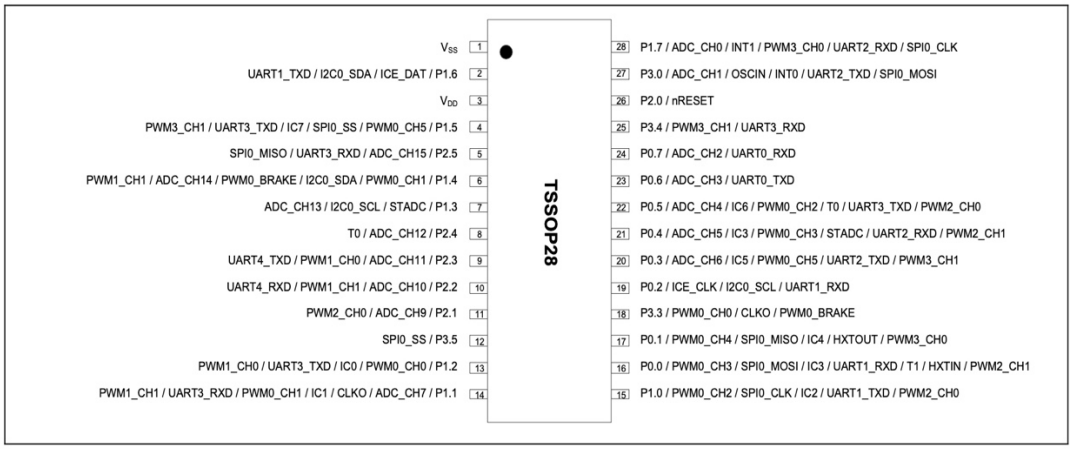
	• 10 kHz low-speed internal oscillator (LIRC) calibrating to ±1% by software from high-speed internal oscillator
Timers	
16-bit Timer	• Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051. • One 16-bit Timer2 with three-channel input capture module and 9 input pin can be selected. • One 16-bit auto-reload Timer3, which can be the baud rate clock source of UART0 and UART1.
Watchdog	• 6-bit free running up counter for WDT time-out interval. • Selectable time-out interval is 6.40 ms ~ 1.638s since WDT_CLK = 10 kHz (LIRC). • Able to wake up from Power-down or Idle mode • Interrupt or reset selectable on watchdog time-out
Wake-up Timer	• 16-bit free running up counter for time-out interval. • Clock sources from LIRC • Able self Wake-up wake up from Power-down or Idle mode, and auto reload count value. • Supports Interrupt
PWM	• Up To 12 output pins can be selected • Supports maximum clock source frequency up to 24 MHz • Supports up to Three PWM modules, each module provides 6 output channels. • Supports independent mode for PWM output • Supports complementary mode for 3 complementary paired PWM output channels • Dead-time insertion with 8-bit resolution • Supports 16-bit resolution PWM counter • Supports mask function and tri-state enable for each PWM pin • Supports brake function • Supports trigger ADC on the following events
Analog Interfaces	
Analog-to-Digital Converter (ADC)	• Analog input voltage range: 0 ~ AV_{DD}. • 12-bit resolution and 10-bit accuracy is guaranteed. • Up to 8 single-end analog input channels • 1 internal channels, they are band-gap voltage (VBG). • Maximum ADC peripheral clock frequency is 1 MHz.

	• Up to 500 KSPS sampling rate. • Software Write 1 to ADCS bit. • External pin (STADC) trigger • PWM trigger. • Support continues convert function auto store the A/D conversion result in XRAM.
Communication Interfaces	
UART	• Supports up to 2 UARTs: UART0, UART1, • Up to three sets ISO 7816-3 device configuration as UART • UART baud rate clock from HIRC or HXT. • Full-duplex asynchronous communications • Programmable 9th bit. • TXD and RXD pins of UART0 exchangeable via software.
I^{2}C	• 1 sets of I^{2}C devices • Master/Slave mode • Bidirectional data transfer between masters and slaves • 7-bit addressing mode • Standard mode (100 kbps) and Fast mode (400 kbps). • Supports 8-bit time-out counter requesting the I^{2}C interrupt if the I^{2}C bus hangs up and timer-out counter overflows • Supports hold time programmable
SPI	• 1 sets of SPI devices • Supports Master or Slave mode operation • Supports MSB first or LSB first transfer sequence • slave mode up to 12 MHz
ISO-7816	• Up to three sets ISO 7816-3 device • Supports ISO 7816-3 compliant T=0, T=1 • Supports full-duplex UART mode.
GPIO	• Four I/O modes: • Quasi-bidirectional mode • Push-Pull Output mode • Open-Drain Output mode • Input only with high impendence mode • Schmitt trigger input / TTL mode selectable. • Each I/O pin configured as interrupt source with edge/level trigger setting

	• Standard interrupt pins $\overline{INT0}$ and $\overline{INT1}$. • Supports high drive and high sink current I/O • I/O pin internal pull-up or pull-down resistor enabled in input mode. • Maximum I/O Speed is 24 MHz • Enabling the pin interrupt function will also enable the wake-up function
ESD & EFT	
ESD	• HBM pass 8 kV
EFT	• > ± 4.4 kV
Latch-up	• 150 mA pass

TSSOP 28-pin Package Pin Diagram

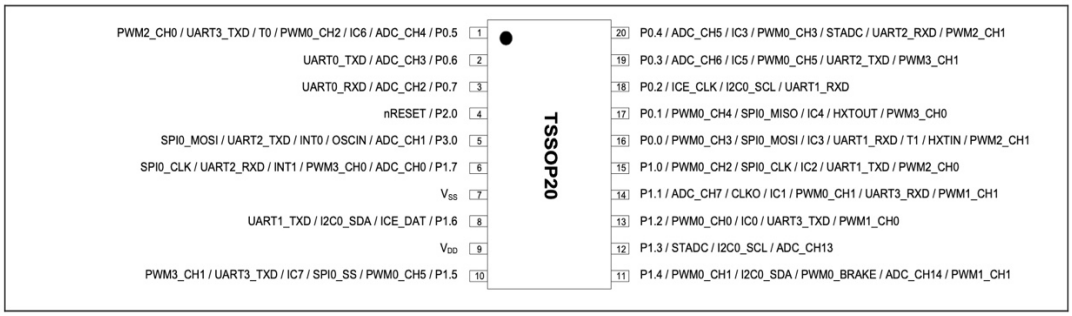
Corresponding Part Number: Q8F203C32-SS28



Pin Assignment of TSSOP28 Package

TSSOP 20-pin Package Pin Diagram

Corresponding Part Number: Q8F202C32-SS20



Pin Assignment of TSSOP20 Package

1 APPLICATION CIRCUIT

1.1 Power supply scheme

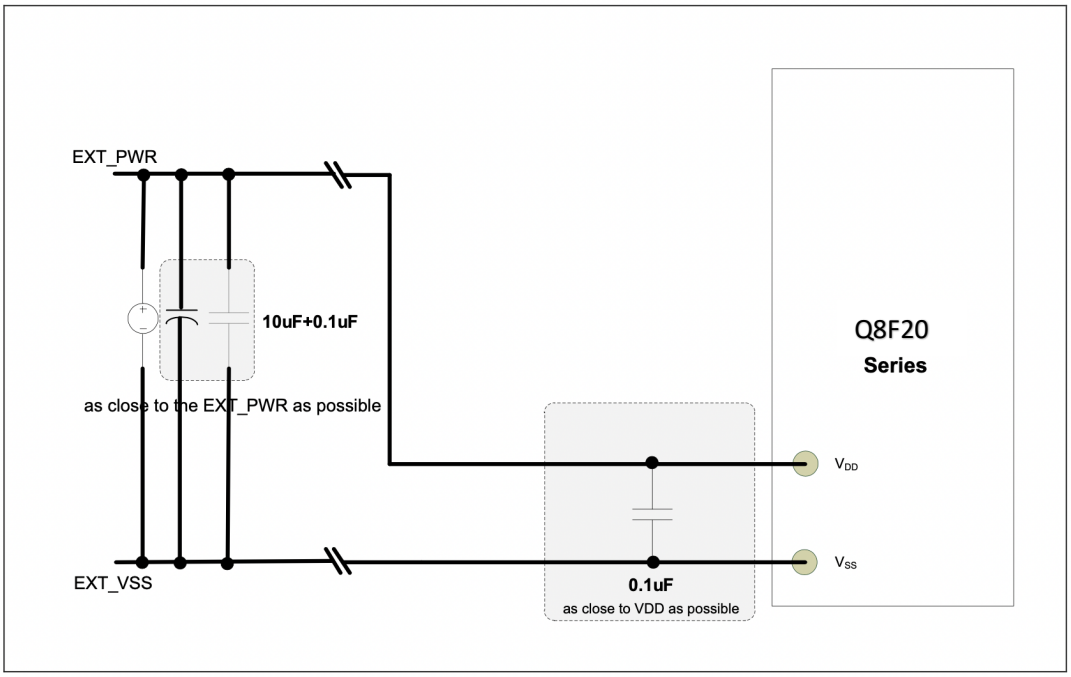
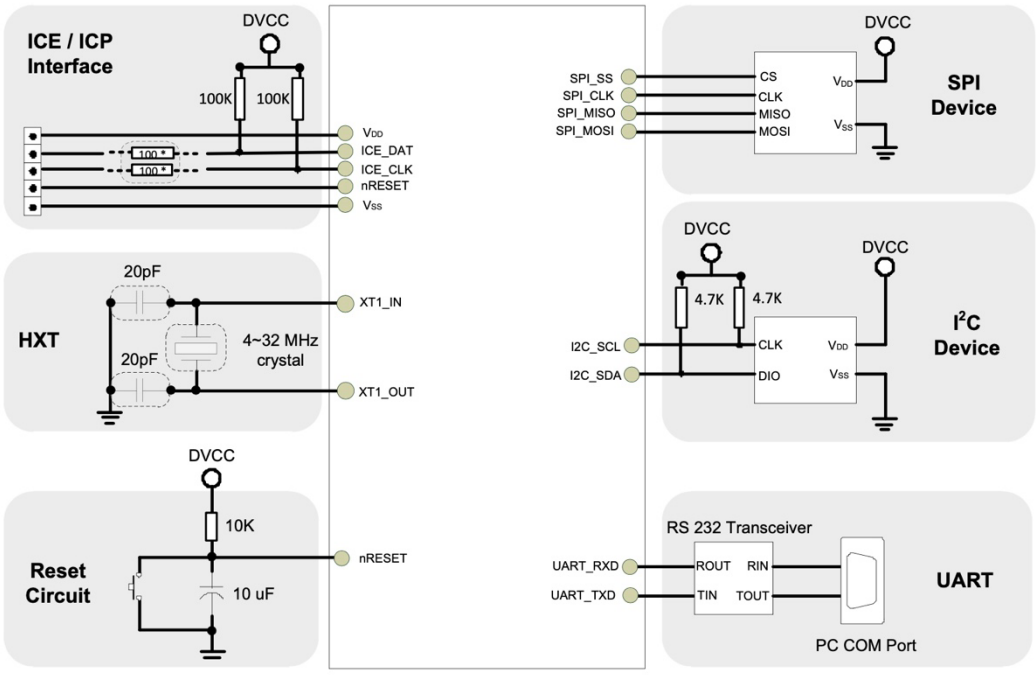


Figure 1-1 Power supply circuit

2 Peripheral Application scheme



*ICE/ICP interface ICE_DAT/ICE_CLK pin 100ohm resister is selectable only for filter the disturb of noise on the circuit.

Note:

1. It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.
2. It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
3. It is optional add 100ohm resistor series between ICE_DAT/ICE_CLK pin to help filtering noise interference.
4. The HXT external capacitor value please reference Section Typical Crystal Application Circuits Capacitors Value

Figure 2-1 Peripheral interface circuit

3 ELECTRICAL CHARACTERISTICS

Please refer to the relative Datasheet for detailed information about the electrical characteristics.

3.1 General Operating Conditions

(V_{DD}-V_{SS} = 2.4 ~ 5.5V, T_A = 25°C, Fsys = 16 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operation voltage	2.4	-	5.5	V	
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{BG}	Band-gap voltage[2]	1.17	1.22	1.30		T_A = 25 °C
		1.14		1.33		T_A = -40°C ~105 °C,

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. Based on characterization, tested in production.

Table 3.1-1 General operating conditions

3.2 DC Electrical Characteristics

3.2.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 2.4V ~ 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals clock base is the system clock Fsys.
- Program run "while (1);" in Flash.

Symbol	Conditions	Fsys	Typ [6]	Max[6][7]			Unit
			T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable	24 MHz(HIRC)[1] @5.5V	3.6	4.2	4.6	4.8	mA
		24 MHz(HIRC)[1] @3.3V	3.2				
		24 MHz(HIRC)[1] @2.4V	2.9				
		16 MHz (HIRC) [1] @5.5V	3.3	3.4	3.9	4.6	
		16 MHz (HIRC) [1] @3.3V	3.1				
		16 MHz (HIRC) [1] @2.4V	2.8				
		10 kHz (LIRC)[2]	0.30	0.32	0.46	2.33	

Notes:

1. This value base on HIRC enable, LIRC enable
2. This value base on HIRC disable, LIRC enable
3. LVR17 enabled, POR enable and BOD enable.
4. Based on characterization, not tested in production unless otherwise specified.

Table 3.2-1 Current consumption in Normal Run mode

Symbol	Conditions	Fsys	Typ [3]	Max[3][4]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, executed from Flash, all peripherals disable	24 MHz(HIRC)[1] @5.5V	2.8	2.9	3.2	3.8	mA
		24 MHz(HIRC)[1] @3.3V	2.4				
		24 MHz(HIRC)[1] @2.4V	2.2				
		16 MHz (HIRC)[1] @5.5V	2.2	2.5	2.6	3.2	
		16 MHz (HIRC)[1] @3.3V	1.9				
		16 MHz (HIRC)[1] @2.4V	1.8				
		10 kHz (LIRC)[2]	0.3	0.5	0.9	2.3	

Notes:
1. This value base on HIRC enable, LIRC enable
2. This value base on HIRC disable, LIRC enable
3. LVR17 enabled, POR enable and BOD enable.
4. Based on characterization, not tested in production unless otherwise specified.

Table 3.2-2 Current consumption in Idle mode

Symbol	Test Conditions	Typ[1]	Max[2]			Unit
		T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_PD}	Power down mode, all peripherals disable@5.5V	6.5	6.2	9	55	µA
	Power down mode, all peripherals disable@3.3V	6				
	Power down mode, all peripherals disable@2.4V	5.8				
	Power down mode, LVR enable all other peripherals disable	7.5	6.7	10[3]	57	
	Power down mode, LVR enable BOD enable all other peripherals disable	180	165	197	292	

Notes:
1. AV_{DD} = V_{DD} = 3.3V unless otherwise specified, LVR17 disabled, POR disabled and BOD disabled.
2. Based on characterization, not tested in production unless otherwise specified.
3. Based on characterization, tested in production.

Table 3.2-3 Chip Current Consumption in Power down mode

3.2.2 Wakeup Time from Low-Power Modes

Symbol	Parameter		Typ	Max	Unit
t_{WU_IDLE}[1]	Wakeup from IDLE mode		5	6	cycles
t_{WU_NPD}[2][3]	Wakeup from Power down mode	Fsys = HIRC @16MHz	-	30	μs
		Fsys = HIRC @ 24MHz		30	μs

Notes:
1. Measured on a wakeup phase with a 16 MHz HIRC oscillator.
2. Based on test during characterization, not tested in production.
3. The wakeup times are measured from the wakeup event to the point in which the application code reads the first.

Table 3.2-4 Low-power mode wakeup timings

3.2.3 I/O DC Characteristics

3.2.3.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage	0	-	$0.3*V_{DD}$	V	
V_{IL1}	Input low voltage (I/O with TTL input)	V_{SS}-0.3	-	$0.2V_{DD}$-0.1	V	
V_{IH}	Input high voltage	$0.2V_{DD}$+0.9	-	V_{DD}+0.3	V	
V_{IH1}	Input high voltage (I/O with Schmitt trigger input and Xin)	$0.7*V_{DD}$	-	V_{DD}	V	
V_{HY}[1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[2]	Input leakage current	-1		1	μA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1		1		$V_{DD} < V_{IN} < 5.5$ V, Open-drain or input only mode

Notes:
1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.
3. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up resistors must be disabled. Leakage could be higher than the maximum value, if positive current is injected on adjacent pins

Table 3.2-5 I/O input characteristics

3.2.3.2 I/O Output Characteristics

The minimum and maximum values are obtained for V_{DD} = 2.4V ~ 5.5 V and temperature condition is T_A= 25 °C unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[1] [2]	Source current for quasi-bidirectional mode and high level	-7.4	-	-7.5	μA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-7.3	-	-7.5	μA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-7.3	-	-7.5	μA	V_{DD} = 2.4 V V_{IN} =(V_{DD}-0.4) V
		-57.2	-	-58.3	μA	V_{DD} = 5.5 V V_{IN} = 2.4 V
	Source current for push-pull mode and high level	-9	-	-9.6	mA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-6	-	-6.6	mA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-4.2	-	-4.9	mA	V_{DD} = 2.7 V V_{IN} =(V_{DD}-0.4) V
		-18	-	-20	mA	V_{DD} = 5.5 V V_{IN} = 2.4 V
I_{SK}[1] [2]	Sink current for push-pull mode and low level	18	-	20	mA	V_{DD} = 5.5 V V_{IN} = 0.4 V
		16	-	18	mA	V_{DD} = 3.3 V V_{IN} = 0.4 V
		9.7	-	12.5	mA	V_{DD} = 2.4 V V_{IN} = 0.4 V
V_{OH}[1]	Output high level voltage for quasi-bidirectional mode	V_{DD}-0.4	-	V_{DD}	V	I_{SR} = -7.3 uA
	Output high level voltage for push-pull mode	V_{DD}-1.2	-	V_{DD}	V	V_{DD} ≥ 4.5 V I_{SR} = -20 mA
					V	V_{DD} ≥ 3.3 V I_{SR} = -13 mA
					V	V_{DD} ≥ 2.7 V I_{SR} = -9 mA
		V_{DD}-0.4	-	V_{DD}	V	V_{DD} ≥ 4.5 V I_{SR} = -9 mA
					V	V_{DD} ≥ 3.3 V I_{SR} = -6 mA
					V	V_{DD} ≥ 2.7 V I_{SR} = -4.2 mA

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}[1]	Output low level voltage for push-pull mode	V_{SS}	-	1.2	V	V_{DD} ≥ 2.7 V I_{SR} = 20 mA (Max.)
		V_{SS}	-	0.4	V	V_{DD} ≥ 5.5 V I_{SR} = 18 mA
					V	V_{DD} ≥ 3.3 V I_{SR} = 16 mA
					V	V_{DD} ≥ 2.4 V I_{SR} = 9.7 mA
C_{IO}[1]	I/O pin capacitance	-	5	-	pF	

Notes:
1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 3.2-6 I/O output characteristics

3.2.3.3 *nRESET Input Characteristics*

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[1]	Internal nRESET pull up resistor	45	-	60	KΩ	V_{DD} = 5.5 V
		45	-	65		V_{DD} = 2.4 V
t_{FR}[1]	nRESET input response time	-	1.5	-	μs	Normal run and Idle mode
		10	-	25		Power down mode

Notes:
1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 3.2-7 nRESET Input Characteristics

3.3 AC Electrical Characteristics

3.3.1 Internal High Speed RC Oscillator (HIRC)

3.3.1.1 16MHz RC Oscillator (HIRC)

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	16[1]	-	MHz	T_A = 25 °C, V_{DD} = 3.3
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20 °C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
		-4[4]		4[4]	%	T_A = -40 °C ~ -20 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	μA	
T_S[3]	Stable time	-	3	5	μs	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V

Notes:
1. Default setting value for the product
2. Based on reload value.
3. Based on characterization, tested in production.
4. Guaranteed by characterization result, not tested in production.
5. Guaranteed by design.

Table 3.3-1 16 MHz Internal High Speed RC Oscillator(HIRC) characteristics

3.3.1.2 24MHz RC Oscillator (HIRC)

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	24[1]	-	MHz	T_A = 25 °C, V_{DD} = 3.3
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20°C ~ +85 °C, V_{DD} = 2.4 ~ 5.5V
		-4[4]		4[4]	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	μA	
T_S[3]	Stable time	-	3	5	μs	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V

Notes:
1. Default setting value for the product
2. Based on reload value.
3. Based on characterization, tested in production.
4. Guaranteed by characterization result, not tested in production.
5. Guaranteed by design.

Table 3.3-2 24MHz Internal High Speed RC Oscillator(HIRC) characteristics

3.3.2 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[1]	Typ	Max[1]	Unit	Test Conditions[2]
V_{DD}	Operating voltage	1.8	-	5.5	V	
R_f	Internal feedback resister	-	500	-	kΩ	
f_{HXT}	Oscillator frequency	4	-	24	MHz	
I_{HXT}	Current consumption	-	80	180	μA	4 MHz, Gain = L0
		-	110	300		8 MHz, Gain = L1
		-	180	500		12 MHz, Gain = L2
		-	230	650		16 Mhz, Gain = L3
		-	360	975		24 MHz, Gain = L4
T_S	Stable time	-	3500	3700	μs	4 MHz, Gain = L0
		-	950	1050		8 MHz, Gain = L1
		-	700	850		12 MHz, Gain = L2
		-	450	550		16 Mhz, Gain = L3
		-	400	570		24 MHz, Gain = L4
Du_{HXT}	Duty cycle	40	-	60	%	

Notes:
1. Guaranteed by characterization, not tested in production.
2. L0 ~ L4 defined by SFR XLTCON[6:4] HXSG

Table 3.3-3 External 4~24 MHz High Speed Crystal (HXT) Oscillator

3.3.2.2 Typical Crystal Application Circuits Capacitors Value

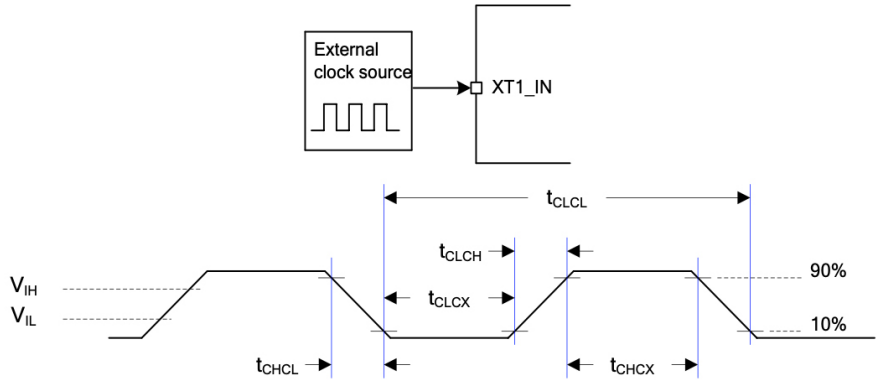
For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 25 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 24 MHz	10 ~ 25 pF	10 ~ 25 pF	without

3.3.3 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	4	-	24	MHz	
t_{CHCX}	Clock high time	8	-	-	ns	
t_{CLCX}	Clock low time	8	-	-	ns	
t_{CLCH}	Clock rise time	-	-	10	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	ns	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:
1. Guaranteed by characterization, not tested in production.

Table 3.3-4 External 4~24 MHz High Speed Clock Input Signal

3.3.4 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{LRC}	Oscillator frequnecy	-	10	-	kHz	
	Frequency drift over temperarure and volatge	-10[1]	-	10[1]	%	T_A = 25 °C, V_{DD} = 5V
		-35[2]	-	35[2]	%	T_A=-40~105°C Without software calibration
I_{LRC}[3]	Operating current	-	0.85	1	μA	V_{DD} = 3.3V
T_S	Stable time	-	500	-	μs	T_A=-40~105°C

Notes:
1. Guaranteed by characterization, tested in production.
2. Guaranteed by characterization, not tested in production.
3. Guaranteed by design.

Table 3.3-5 10 kHz Internal Low Speed RC Oscillator(LIRC) characteristics

3.3.5 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Normal mode [4] output high (90%) to low level (10%) falling time	4.6	5.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.9	3.3		C_L = 10 pF, V_{DD} >= 5.5 V
		6.6	8		C_L = 30 pF, V_{DD} >= 3.3 V
		4.3	5		C_L = 10 pF, V_{DD} >= 3.3 V
		8.5	12.5		C_L = 30 pF, V_{DD} >= 2.4 V
		8.0	10.7		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{f(IO)out}$	High slew rate mode [5] output high (90%) to low level (10%) falling time	4.0	4.3	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		4.9	5.8		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		9.5	13.8		C_L = 30 pF, V_{DD} >= 2.4 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	Normal mode [4] output low (10%) to high level (90%) rising time	5.6	6.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		3.4	3.7		C_L = 10 pF, V_{DD} >= 5.5 V
		8.1	9.4		C_L = 30 pF, V_{DD} >= 3.3 V
		5.1	5.8		C_L = 10 pF, V_{DD} >= 3.3 V
		15.1	20.3		C_L = 30 pF, V_{DD} >= 2.4 V
		9.6	12.4		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	High slew rate mode [5] output low (10%) to high level (90%) rising time	4.8	5.2	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		6.4	7.4		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		12.7	16.9		C_L = 30 pF, V_{DD} >= 2.4 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 2.4 V
$f_{max(IO)out}$[*3]	I/O maximum frequency	24	24	MHz	C_L = 30 pF, V_{DD} >= 2.4 V
					C_L = 10 pF, V_{DD} >= 2.4 V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. PxSR.n bit value = 0, Normal output slew rate
5. PxSR.n bit value = 1, high speed output slew rate

Table 3.3-6 I/O AC characteristics

3.4 Analog Characteristics

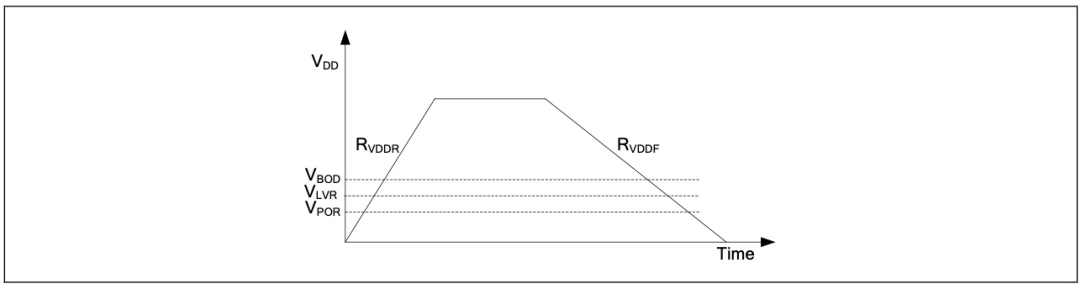
3.4.1 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	10		20	μA	AV_{DD} = 5.5V
I_{LVR}[*1]	LVR operating current	0.5	-	1		AV_{DD} = 5.5V
I_{BOD}[*1]	BOD operating current	-	0.5	2.9		AV_{DD} = 5.5V
V_{POR}	POR reset voltage	1	1.15	1.3	V	-
V_{LVR}	LVR reset voltage	1.7	2.0	2.4		-
V_{BOD}	BOD brown-out detect voltage	4.10	4.4	4.70		BOV[1:0] = [0,0]
		3.50	3.7	3.90		BOV[1:0] = [0,1]
		2.50	2.7	2.90		BOV[1:0] = [1,0]
		2.00	2.2	2.40		BOV[1:0] = [1,1]
T_{LVR_SU}[*1]	LVR startup time	60	-	80	μs	-
T_{LVR_RE}[1]	LVR respond time	0.4	-	4		Fsys = HIRC@16MHz
		180	-	350		Fsys = LIRC
T_{BOD_SU}[1]	BOD startup time	180	-	320		Fsys = HIRC@16MHz
T_{BOD_RE}[1]	BOD respond time	2.5	-	5		Fsys = HIRC@16MHz

Notes:
1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 3.4-1 Reset and power control unit



BODFLT (BODCON1.1)	BOD Operation Mode	System Clock Source	Minimum Brown-out Detect Pulse Width
0	Normal mode (LPBOD[1:0] = [0,0])	Any clock source	Typ. 1μs
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	16 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	64 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	256 ($1/F_{LIRC}$)
1	Normal mode (LPBOD[1:0] = [0,0])	HIRC/ECLK	Normal operation: 32 ($1/F_{SYS}$) Idle mode: 32 ($1/F_{SYS}$) Power-down mode: 2 ($1/F_{LIRC}$)
		LIRC	2 ($1/F_{LIRC}$)
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	18 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	66 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	258 ($1/F_{LIRC}$)

Table 3.4-2 Minimum Brown-out Detect Pulse Width

3.4.2 12-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	2.7	-	5.5	V	$AV_{DD} = V_{DD}$
V_{REF}	Reference voltage	2.7	-	AV_{DD}	V	$V_{REF} = AV_{DD}$
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	Operating current (AV_{DD} + V_{REF} current)	-	-	418	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 5.5 V F_{ADC} = 500 kHz T_{CONV} = 17 * T_{ADC}
N_R	Resolution	12			Bit	
F_{ADCEC}[1]	Encoding Rate	500			kHz	This value is fixed by ADC module
T_{ADCEC}	Encoding Time	2			μs	This value is fixed by ADC module
F_{ADCSMP}[1]	ADC Sampling Clock frequency	F_{SYS}/8		F_{SYS}	kHz	base on ADCDIV (ADCCON1[5:4]
T_{ADCSMP}	ADC Sampling Time [2]z	0.375	-	17	μs	F_{SYS} = 16MHz;
		0.417	-	11.3	μs	Fsys = 24MHz; ADCAQT = 1 by software[3]
F_{ADCCOV}	Conversion Rate $F_{ADCCOV} = 1/T_{ADCCOV}$	52.6	-	421	kHz	F_{SYS} = 16MHz;
		75.2	-	413	kHz	F_{SYS} = 24MHz;
T_{ADCCOV}[2]	Conversion Time $T_{ADCCOV} = T_{SMP} + T_{ADCEC}$	2.375	-	19	μs	F_{SYS} = 16MHz;
		2.417	-	13.3	μs	F_{SYS} = 24MHz;
T_{ADCEN}	ADC Enable to ready time	20	-	-	μs	
INL[1]	Integral Non-Linearity Error	-3	-	+3	LSB	$V_{REF} = AV_{DD} = V_{DD}$
DNL[1]	Differential Non-Linearity Error	-2	-	+4	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_G[1]	Gain error	-3.5	-	+0.4	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_O[1]$_T$	Offset error	-2	-	+2.8	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_A[1]	Absolute Error	-7	-	+7	LSB	$V_{REF} = AV_{DD} = V_{DD}$
R_S	Input Channel Equivalent Resistance	-	0.5	2.5	kΩ	
C_{IN}	Input Equivalent Capacitance	-	2.5	-	pF	

1. Guaranteed by characterization result, not tested in production.
2. ADC Convertion time T_{ADCCOV} = ADC Sampling Time (T_{SMP}) + ADC Encoding Time (T_{ADCEC}).
3. ADC Sampling Time $T_{SMP} = \frac{4 * ADCAQT + 6}{F_{ADCSMP}}$ （F_{ADCSMP} base on ADCDIV (ADCCON1[5:4])

   If F_{SYS} = 16MHz, ADC Sampling Time Minimum condition $\frac{6}{16MHz}$ (ADCAQT = 0, ADCDIV = 0), ADC Sampling Time Maximum condition $\frac{4*7+6}{16MHz/8}$ (ADCAQT = 7, ADCDIV = 8)

   If F_{SYS} = 24MHz, ADC Sampling Time Minimum condition $\frac{4*1+6}{24MHz}$ (ADCAQT = 1, ADCDIV = 0), Since the minimum sampling time must over 370ns that means when F_{ADCAQT} = 24MHz, ADCAQT must be set as 1 by software at least.

3.7 Absolute Maximum Ratings

Volrage Stesses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

3.7.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	6.5	V
ΔV_{DD}	Variations between different power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on I/O	V_{SS}-0.3	5.5	V

Notes:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.

Table 3.7-1 Voltage characteristics

3.7.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	200	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	200	
I_{IO}	Maximum current sunk by a I/O Pin	-	22	
	Maximum current sourced by a I/O Pin	-	10	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by V_{IN}>A_{VDD} and a negative injection is caused by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 3.7-2 Current characteristics

3.7.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (°C)
- θ_{JA} = thermal resistance junction-ambient (°C/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	°C
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 20-pin QFN(3x3 mm)	-	68	-	°C/Watt
	Thermal resistance junction-ambient 20-pin TSSOP(4.4x6.5 mm)	-	38	-	°C/Watt
	Thermal resistance junction-ambient 28-pin TSSOP(4.4x9.7 mm)		30	-	°C/Watt
	Thermal resistance junction-ambient 32-pin LQFP(7x7 mm)		62	-	°C/Watt
	Thermal resistance junction-ambient 33-pin QFN(4x4 mm)		28	-	°C/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 3.7-3 Thermal characteristics

3.7.4 EMC Characteristics

3.7.4.1 Electrostatic discharge (ESD)

For the MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

3.7.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

3.7.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-8000	-	+8000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-1000	-	+1000	
LU[*3]	Pin current for latch-up[*3]	-400	-	+400	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

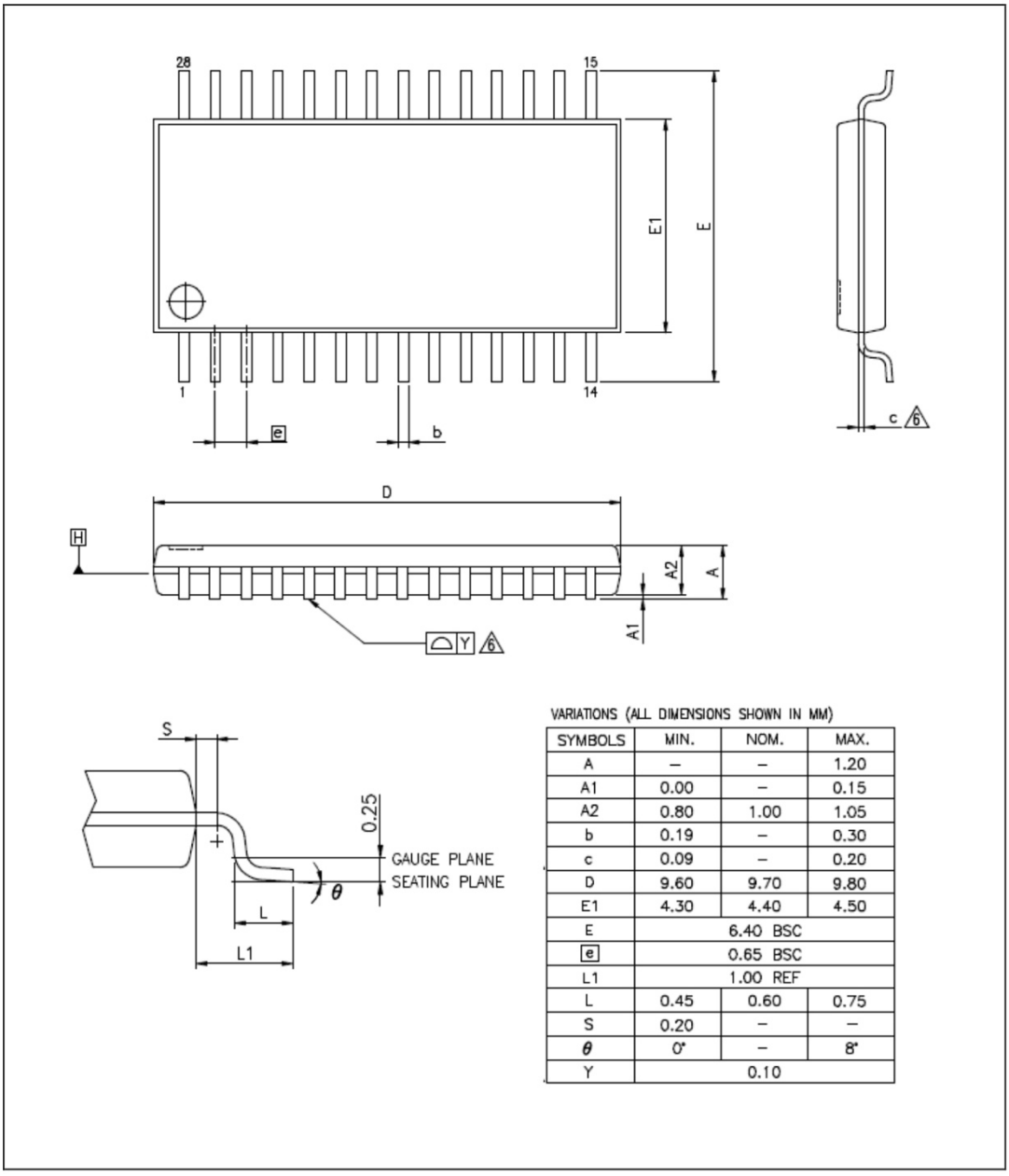
Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 3.7-4 EMC characteristics

9 PACKAGE DIMENSIONS

TSSOP 28-pin (4.4 x 9.7 x 1.0 mm)

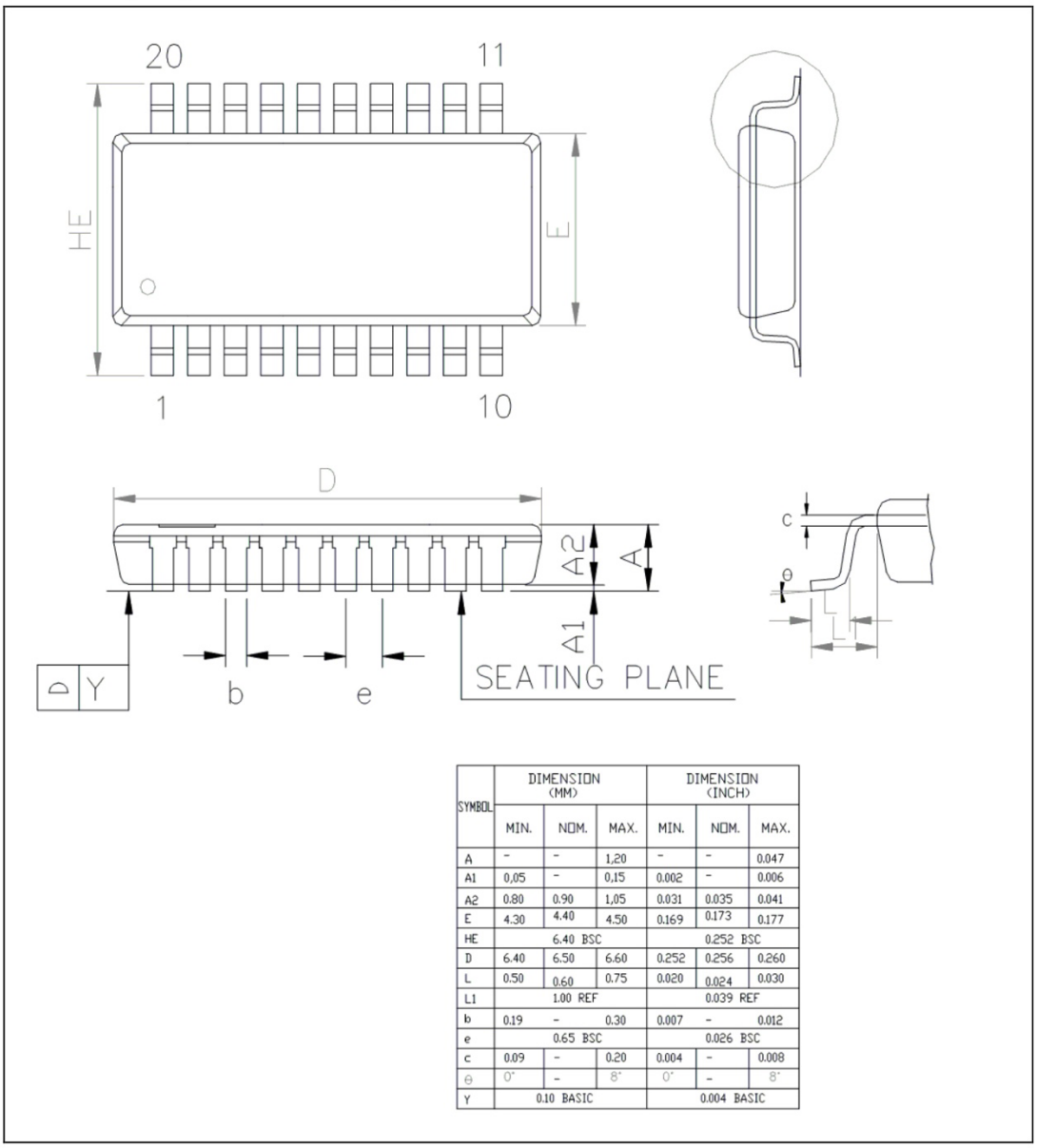


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°
Y	0.10		

TSSOP-28 Package Dimension

TSSOP 20-pin (4.4 x 6.5 x 0.9 mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	-	0.30	0.007	-	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y	0.10 BASIC			0.004 BASIC		

TSSOP-20 Package Dimension